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10/643,665	08/19/2003	John Malvern Swope	200205326-1	5751

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/643,665	SWOPE, JOHN MALVERN	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/643,665 filed 08/19/2003 and amendment filed 01/24/2006.

2. Claims 1-22 remain pending in the Application.

3. Applicant's arguments with respect to the rejection of claims 1-22 under 35 USC § 102 (e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Chang et al. (US Patent 5,546,321).

Claim Objections

4. Claims 1, 13 and 18 are objected to because of the following informalities:

Claim 1 line 2 after "one" delete "of" insert –or--

Claim 13 line 5 after "one" delete "of" insert –or--

Claim 18 line 3 after "one" delete "of" insert –or--

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is indefinite if the step of "generate the low level details" is performed in an iterative mode as claimed (claims 1, 13 and 18) while Specification of the instant Application states on the page 3 lines 19-23: ". . . a printed

circuit board (PCB) design module is configured to receive high level constraints associated with a desired PCB from a user and generate low level details that comprise a printed circuit board design". Therefore claims 1, 13 and 18 fail to define the sequence of the steps of generating a printed circuit board design module to present the invention clearly. Moreover it is not clear how a generation of **low level details** is performed in a **third limitations** based on the high level constraints determined in the second limitation to **generate low level details**, while the **low level details** have been derived in the **first limitation** (claims 1, 13 and 18) already. It has to be noted that rejection of claims 1-22 under 35 USC § 112 has been done **twice.** Therefore it creates a basis for finality of rejecting claims 1-22.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. (US Patent 5,546,321).

With respect to claims 1 and 18 Chang et al. teaches a method for generating a printed circuit board design module design tool an a method of fabricating a multi-layer printed circuit board (abstract); a computer-readable medium storing a printed circuit board design module executable by a computer system, where the printed circuit board design module is generated within an intelligent computer program called an expert

system (col. 1, ll.48-50) performing sequential process for printed circuit design in sequence, such as the initial deign derived from the customer specification is then subjected to a cost engineering analysis, a reliability analysis and a manufacturability analysis (col. 1, ll.28-33), comprising: compiling information that is usable to derive one or more low level details associated with a printed circuit board within expert system shown on the Fig. 9, which uses as input an information from a user related to the printed circuit design including qualified design and chip parameter database (col. 14, ll.50-51), wherein the database contain the information of PCB physical dimensions (low level detail) (col. 11, ll.58-63); determining one or more high level constraints that are usable with the information to generate the low level details subsequent to compiling the information as shown on the Figs. 8 and 9 expert system computes the electrical parameters of PCB cross section (high level constraints) using fitting algorithm (col. 14, ll.36-38; col. 9, ll.60-67); and subsequent to determining the one or more high level constraint, generating the printed circuit board design module such that the printed circuit board design module includes the information and such that the printed circuit board design module is configured to receive the one or more high level constraints and generate the low level details using the information in response to receiving the one or more high level constraints within designing multilayer PCB (cross section) (col. 8, ll.35-45) using expert system to use previously qualified products, PCB cross section dimensions, etc. to produce parameters (constraints) for PCB design as shown on the Fig. 9.

With respect to claim 13 Chang et al. teaches a computer system within CAD tools, which is computer system (col. 17, ll.37-43), comprising: a processor within ability the system used for generating printed circuit design to execute of program instructions (col. 17, ll.15-18); and a memory that includes a printed circuit board design module that is executable by the processor within saving (i.e. storing in the memory) a result of steps performed by expert system to design printed circuit module as shown on the Fig. 13 (col. 15, ll.55-57), the printed circuit board design module being generated by: compiling information that is usable to derive one of more low level details associated with a printed circuit board within expert system shown on the Fig. 9, which uses as input an information from a user related to the printed circuit design including qualified design and chip parameter database (col. 14, ll.50-51), wherein the database contain the information of PCB physical dimensions (low level detail) (col. 11, ll.58-63); determining one or more high level constraints that are usable with the information to generate the low level details subsequent to compiling the information as shown on the Figs. 8 and 9 expert system computes the electrical parameters of PCB cross section (high level constraints) using fitting algorithm (col. 14, ll.36-38; col. 9, ll.60-67); and subsequent to determining the one or more high level constraint generating the printed circuit board design module such that the printed circuit board design module includes the information and such that the printed circuit board design module is configured to receive the one or more high level constraints and generate the low level details using the information in response to receiving the one or more high level constraints within designing multilayer PCB (cross section) (col. 8, ll.35-45) using expert system to use

previously qualified products, PCB cross section dimensions, etc. to produce parameters (constraints) for PCB design as shown on the Fig. 9.

With respect to claims 2-12, 14-17 and 19-22 Chang et al. teaches:

Claim 2: generating a list of the low level details prior to compiling the information within a database storing the data of the printed circuit board geometry as a result of a regression analysis of the input data having physical dimensions of PCB design (col. 11, ll.58-63);

Claim 3: wherein the high level constraints include schematic constraints within defining design goals as shown on the Figs. 9 and 11 including structural representation as PCB cross sections shown on the Fig. 10 with additional tables 1 and 2 as an example (col. 10, ll.33-67);

Claim 4: wherein the high level constraints include electrical constraints within defining design goals as shown on the Figs. 9 and 11 including calculated electrical parameters of the PCB design by fitting algorithm (col. 10, ll.5-7; ll.20-23; col. 8, ll.36-44);

Claim 5: wherein the high level constraints include mechanical constraints within defining design goals as shown on the Figs. 9 and 11 including specifying cost, manufacturing and reliability constraints specified as shown on the Fig. 9 (col. 16, ll.9-11);

Claim 6: wherein the high level constraints include cost constraints within defining design goals as shown on the Fig. 11 including specifying cost, manufacturing and reliability constraints specified as shown on the Fig. 9 (col. 16, ll.9-11);

Claim 7: wherein the low level details include routing details within inputting the data into expert system for further processing, such as PCB design geometry including wiring grids, geometrical dimensions etc. (col. 8, ll.64-67; col. 7, ll.1-7);

Claim 8: wherein the low level details include component placement details within inputting the data into expert system for further processing, such as PCB design geometry including wiring grids, geometrical dimensions etc. (col. 8, ll.64-67; col. 7, ll.1-7);

Claim 9: wherein the low level details include stack-up details within inputting the data into expert system for further processing, such as PCB design geometry including wiring grids, geometrical dimensions etc. (col. 8, ll.64-67; col. 7, ll.1-7);

Claims 10, 14, 19: wherein the information includes mathematical equations usable to calculate the low level details using the high level constraints as shown in column 12, wherein calculation of low level details is demonstrated by using a various of equations and using backward mode including recommendations for the design alternatives (col. 8, ll.63-67);

Claims 11, 15, 20: wherein the information includes a table usable to determine the low level details using the high level constraints within qualified design and chip parameter database as shown on the Fig. 8 (col. 14, ll.49-53; ll.56-59) using input variables (col. 15, ll.5-7) and relationships to obtain output variables for modifying low level details for PCB design (col. 15, ll.29-33);

Claim 12: generating the printed circuit board design module such that the printed circuit board design module is configured to receive the one or more high level

constraints from a user interface incorporated into a schematic software tool within the method and system having an ability to reconcile the product design parameters with testability constraints of each test plan (col. 17, ll.7-12; ll.26-31);

Claim 16: wherein the high level constraints are selected from the group consisting of schematic constraints within defining design goals as shown on the Figs. 9 and 11 including structural representation as PCB cross sections shown on the Fig. 10 with additional tables 1 and 2 as an example (col. 10, ll.33-67), electrical constraints within defining design goals as shown on the Figs. 9 and 11 including calculated electrical parameters of the PCB design by fitting algorithm (col. 10, ll.5-7; ll.20-23; col. 8, ll.36-44), and mechanical constraints within defining design goals as shown on the Figs. 9 and 11 including specifying cost, manufacturing and reliability constraints specified as shown on the Fig. 9 (col. 16, ll.9-11);

Claims 17, 22: wherein the low level details are selected from the group consisting of routing details, component placement details, and stack up details within inputting the data into expert system for further processing, such as PCB design geometry including wiring grids, geometrical dimensions etc. (col. 8, ll.64-67; col. 7, ll.1-7);

Claim 21: wherein the high level constraints are selected from the group consisting of schematic constraints, electrical constraints, and mechanical constraints within defining design goals as shown on the Figs. 9 and 11 including structural representation as PCB cross sections shown on the Fig. 10 with additional tables 1 and 2 as an example (col. 10, ll.33-67); including calculated electrical parameters of the

PCB design by fitting algorithm (col. 10, ll.5-7; ll.20-23; col. 8, ll.36-44); including specifying cost, manufacturing and reliability constraints specified as shown on the Fig. 9 (col. 16, ll.9-11).

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1-22 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-21 of copending Application No. 10/193,623 (hereinafter '623 Application). Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant Application and copending '623 Application are claiming common subject matter, as follows: a method and system for generating a printed circuit board design module including receiving design description associated with PCB design, determining a high level constraints for generating the printed circuit board design module. The independent claims 1, 13 and 18 of the instant Application correspond to the independent claims 1, 8 and 15 of the '623 Application and dependent claims 2-12, 14-17 and 19-22 of the instant Application correspond to the dependent claims 2-7, 9-14 and 16-21 of the '623 Application. The corresponding claims are different in their wording bur clearly disclose the same material.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

10. Applicant's amendment necessitated the rejection under 35 USC § 112 presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See

MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

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